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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,671	01/17/2002	Amr M. Mohsen	003921.00248	6141

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EXAMINER	
JONES, HUGH M	

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/052,671	MOHSEN, AMR M.	
	Examiner	Art Unit	
	Hugh Jones	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59-72 and 74-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59-72 and 74-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/28/2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 59-72, 74-82 of U.S. Application 10/052,671, filed 01/17/2002 are pending.

Claim Rejections - 35 USC 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 59-72, 74-82 **are rejected under 35 U.S.C. 102(a) as being clearly anticipated by IBM Technical Disclosure (of record).** See pp. 294-299 (especially figs. 6-7). The IBM document discloses interconnected programmable chips on a substrate which are connnected to and configured by another chip or part of a chip. With respect to claims disclosing multiple layers of conductive traces, see pp. 296-297 and fig. 6. With respect to claim limitations concerning discrete elements, see # 5 of page 298.

4. Claims 59-72, 74-82 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Carter (of record).

5. Carter discloses reconfigurable logic. See figure 4a. FIGS. 4A illustrates a configurable logic array containing nine configurable logical elements. As shown in FIG. 4A, each CLE of the nine CLEs 40-1 through 40-9 has a plurality of input

leads and one or more output leads. Each input lead has a plurality of access junctions each connecting a selected general interconnect lead to the input lead. The access junctions for input lead 2 of CLE 40-7 are labeled A1 through A4 in FIG. 4A. The access junctions for the other input leads are indicated schematically but are not labeled for the sake of clarity. Similarly, each output lead of each CLE has a plurality of access junctions each connecting the output lead to a corresponding one of the general interconnect leads.

Response to Arguments

6. Applicants arguments, filed 4/6/2007, have been carefully considered and are not persuasive.

7. Applicants arguments regarding the IBM disclosure and the Carter patent are not persuasive.

8. With respect to the IBM disclosure, Applicants refer to fig. 1. However, the rejection referred to fig. 6-7. Regardless, Applicant's argument is not persuasive. See:

A silicon wiring wafer 1 is used as a carrier for chips 2 and as a chip interconnection means (Fig. 1). The interchip wiring consists of a single or a multi-level grid of wire segments 3 (Fig. 2) on the wiring wafer. The wire segments may be implemented as metal conductor strips, polysilicon type material or even as optical links.

At the ends of wire segments 3, semiconductor switches 4, such as transfer devices in FET technology, are provided (Fig. 3) which permit interconnecting the wire segments 3 and the chip pads. Switches 4 may be dynamically activated for a specific interconnection pattern by master/slave latches 5 located in the wiring wafer. Latches 5 control switches 4 connecting the individual wire segments 3 and may be set by known scan/set mechanisms (such as LSSD or RAS) on request. There-

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Fig. 6-7 are reproduced:

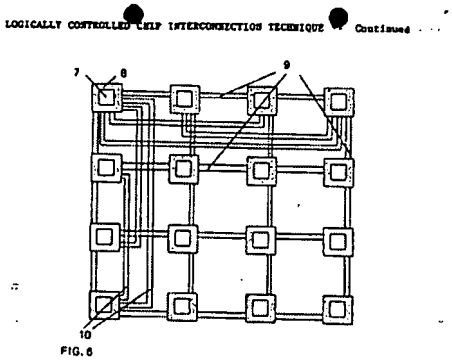

FIG. 6

characteristics, whereas the second metallization layer may be optimized for switches 4 and control latches 5.

Fig. 4 shows the arrangement of switch 4 in FET technology, preferably as a transfer device, and of the associated control latch 5. For the special case where a wiring node is to be used as a wiring dot, the transfer device may be implemented as a common gate (polysilicon/metal) with several diffusion areas at the ends of wire segments 3 (Fig. 5).

A preferred overall implementation of the proposal for 16 VLSI chips in a single silicon wiring wafer is shown in Fig. 6 and has the following major advantages.

1. Each chip site 7 is surrounded by a switch bed 8 consisting of a wire segment matrix with 3 switches at each wiring node.

2. Between the switch beds of each neighboring chip pair, vertical and horizontal direct connection wire channels 9 are implemented.

3. Between each second, third, etc., chip, there are groups of horizontal and vertical wire interconnection channels 10 of the respective length, preferably on separate metallization layers. Such wires end at the respective switch beds 8.

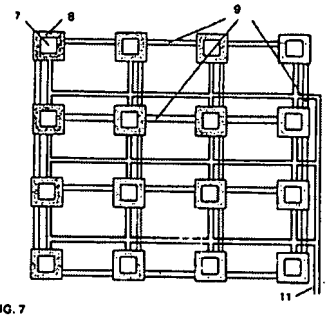

FIG. 7

4. At the crossings of individual horizontal and vertical direct connection wires, single cross switches (transfer devices) may also be realized for possible connection of the horizontal and vertical lines.

   a. Only one cross switch is installed at any end of the direct lines.

   b. For a specific number of direct interconnections, several cross switches are installed at the ends of the direct lines.

   c. For a specific number of direct lines, cross switches are also installed at inner crossings.

5. To improve the electrical signal transmission characteristics, individual integrated decoupling capacitors may be added (dynamically or statically).

6. The threshold voltage at the switches (transfer devices) is chosen higher to meet the low resistance requirements of the switches, particularly since several switches are connected in series in the ultimately interconnected signal transmission path.

9. Applicants argue:

> The Carter patent is directed to a configurable logic element. The Carter patent does not, however, teach or suggest using this element to interconnect a plurality of electrically conductive traces formed on a printed circuit board, as recited in 59-72 and 74-82. Instead, to the extent that the logic element of the Carter patent might be used with a printed circuit board,[2] the purpose of the Carter logic element would seem to be to insert some type of logical operation (e.g., an AND operation, an OR operation, a NOR operation, etc.) between electrically conductive traces, rather than simply connecting them as recited in claims 59-72 and 74-82.

10. Applicant's argument/distinction is not understood.

11. The Kung rejection is withdrawn in order to reduce the number of issues; the arguments are moot.

12. Applicant's arguments regarding the 102 (f, g) rejections are persuasive and they are withdrawn. Applicants are thanked for the arguments.

Conclusion

13. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

14. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (571) 272-3781,

Monday-Thursday 0830 to 0700 ET,

or

the examiner's supervisor, Kamini Shah, telephone number (571) 272-2279.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

or (703) 308-1396 (for informal or draft communications, please label *PROPOSED* or *DRAFT*).

Dr. Hugh Jones
Primary Patent Examiner
July 8, 2007